

# Towards dissipationless topotronics

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Electrical charge transport in traditional nanoscale integrated circuits is always accompanied by energy dissipation in the form of Joule heating, which imposes a thermal bottleneck constraining their performance. The emergence of novel topological systems opens up exciting avenues for optimizing thermal management based on the intuitive concept of “no backscattering, no dissipation”. However, whether energy dissipation can emerge without backscattering inside topological systems remains a question. In this work, we propose a microscopic picture that illustrates energy dissipation in the quantum Hall plateau regime of graphene. Despite the quantization of Hall, longitudinal, and two-probe resistances, we find that the energy dissipation emerges in the form of Joule heat.

In practice, such energy dissipation phenomenon is universal in topological devices, which casts doubt upon whether it is possible to reach truly dissipationless in topotronics. We propose a criterion for judging whether energy dissipation occurs inside a topological device. This criterion establishes a concise algebraic relationship among the number of modes engaged in transport,  $N_{in} = N_{tunl} + N_{bs}$ . We advocate for the indispensability of Chern insulators with higher Chern numbers to achieve functional devices and uphold the no-dissipation rule simultaneously. Our work holds promise for shaping the future of integrated topological circuit designs towards no dissipation.